REMARKS

This Amendment is in response to the Office Action dated February 23, 2005, in which claims 8 and 11-14 are initially rejected, and claims 1-7 and 15-20 were indicated as being directed to allowable subject matter. Applicants would like to thank the Examiner for the indicated allowability of the subject matter recited in claims 1-7, 9-10 and 15-20 and respectfully request reconsideration and allowance of the remaining claims in view of the above-amendments and the following remarks.

I. CLAIM OBJECTIONS

Claims 1 and 5 were objected to because of an informality in the claim language. In particular, the Examiner suggested that the phrase "in a selected arrangement" is not clear. Accordingly, this phrase has been deleted from claims 1 and 15. With this Amendment, Applicants respectfully requests that the objection to claims 1 and 15 be withdrawn.

II. CLAIM REJECTIONS UNDER §103

Claims 8 and 11-14 were rejected under §103(a) as being obvious over Nanda et al., "A New Methodology for the Design of Asynchronous Digital Circuits".

The similarity between the Nanda et al. article and the invention recited in independent claim 8 seems to reside only in the use of a common term, "universal gate". However, the universal gate disclosed by Nanda et al. is quite different in structure and purpose than the universal gate recited in claim 8.

The Nanda et al. article relates to a double-rail logic handshake protocol in which each input and output requires a pair of wires carrying both the data and the handshaking information, as described in the second column on page 342. At the bottom of the same column, Nanda et al. state that, "all responses are edge triggered and are triggered by both the falling and rising edge."

The code has three detectable states: logical 1, logical 0 and a null state. These states can be represented by:

00 = acknowledge-null;

01 = data-value logical zero;

10 = data-value logical 1 and

11 = not allowed.

Thus, each of the two wires can have a "1" or a "0" state.

Under section 3, on page 343, Nanda et al. explicitly state that, "It is not possible to use normal level sensitive logic elements such as AND, OR, INVERT to realise equivalent logic blocks for the asynchronous counterparts based on our way of representing data values. This is the motivation for realising the Universal gate proposed here. We show how to render this gate to give the AND, OR, INVERT elements in the NRZ asynchronous paradigm."

A two-input universal gate is shown in FIG. 1 of the Nanda et al. article, which includes two two-rail inputs A0, A1 and B0 and B1 and four single rail outputs M0, M1, M2 and M3. As stated at the bottom of the first column on page 343, the output transitions occur depending on the four possible input combinations "00, 01, 10 and 11".

Claim 8 of the present application recites a universal gate having a first gate performing an anding function having first and second inputs and providing a first output and a second gate performing an oring function having third and forth inputs and providing a second output. The first, second, third and forth inputs are arranged for selectively coupling to respective first and second nets and negations of the first and second nets. The first and second outputs are arranged for selective coupling to a third net and a negation of the third net.

The Office Action suggests, "the inputs [of Nanda et al.] basically receive binary "1" and "0", therefore a net is

connected to receive the "1" input and a negation net is connected to receive the "0". However, Nanda et al. disclose that each wire can have a zero state or a one state (depending on the data). Nanda et al. do not show first and second gates in which the first, second, third and forth inputs are arranged for selectively coupling to respective first and second nets and negations of the first and second nets, and the first and second outputs being arranged for selective coupling to a third net and a negation of the third net. In fact, the Office Action acknowledged that Nanda et al. does not explicitly teach arranging the inputs as claimed.

Since the purposes and structure of the Nanda et al. universal gate is so different than that of the present invention and since Nanda et al. explicitly state that it is not possible to use normal level sensitive logic elements with their structure, it would not have been obvious to a person of ordinary skill in the art to arrange inputs and outputs as described in claim 8 of the present application.

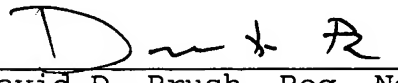
Applicants therefore respectfully request that the rejection of claim 8 and its dependent claims 11-15 be withdrawn.

In addition, dependent claims 11-14 recite further elements and limitations that are neither taught nor suggested by Nanda et al. for example, claim 14 requires the absences of inverters. However, Nanda et al. state that their universal gate can be used to realise a "not" gate.

The Director is authorized to charge any fee deficiency required by this paper or credit any overpayment to Deposit Account No. 23-1123.

Respectfully submitted,

WESTMAN, CHAMPLIN & KELLY, P.A.

By: 

David D. Brush, Reg. No. 34,557
Suite 1600 - International Centre
900 Second Avenue South
Minneapolis, Minnesota 55402-3319
Phone: (612) 334-3222 Fax: (612) 334-3312

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